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PATENTS
MIC-44

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants : Adrian J. Drexler et al.
Application No. : 10/840,015 Confirmation No. : 9647
Filed : May 5, 2004
For : CLOCK CAPTURE IN CLOCK SYNCHRONIZATION
CIRCUITRY
Group Art Unit : 2631
Examiner : Not Yet Assigned

New York, New York 10020
June 1, 2005

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
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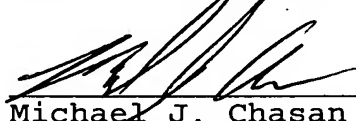
Sir:

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- ☐ [] within three months of the application filing date;
- ☒ [X] more than three months from the application filing
date but before the mailing date of the first Office
Action on the merits.

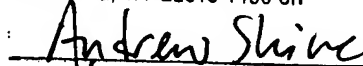
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Respectfully submitted,



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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Applicant Number	10/840,015
Filing Date	May 5, 2004
First Named Inventor	Adrian J. Drexler et al.
Art Unit	2631
Examiner Name	Not Yet Assigned
Attorney Docket Number	MIC-44
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U. S. PATENT DOCUMENT

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		6,556,489 B2	04/29/03	Gomm et al.	
		6,586,979 B2	07/01/03	Gomm et al.	
		6,727,734 B2	04/27/04	Gomm	
		6,735,148 B2	05/11/04	Gomm	
		6,737,897 B2	05/18/04	Gomm et al.	
		6,759,883 B2	07/06/04	Gomm	
		6,774,687 B2	08/10/04	Gomm et al.	
		6,781,861 B2	08/24/04	Gomm et al.	
		6,803,826 B2	10/12/04	Gomm et al.	
		6,850,107 B2	02/01/05	Gomm	

U. S. PUBLISHED DOCUMENT

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		2005/0062510 A1	03/24/05	Zarate et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 2

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	
		Saeki et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, pp. 1656-1668, (1996).
		Shim et al., "An Analog Synchronous Mirror Delay for High-Speed DRAM Application," IEEE Journal of Solid-State Circuits, Vol. 34 No. 4, pp. 484-493, (1999).
		Kim et al., "A Low-Jitter Mixed-Mode DLL for High-Speed DRAM Applications," IEEE Journal of Solid-State Circuits, Vol. 35 No. 10, pp. 1430-1436, (2000).

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